

PTO/SB/08B (08-03)
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Complete if Known

Application Number	09/760,331
Filing Date	January 13, 2001
First Named Inventor	Masatoshi Ishikawa
Art Unit	2625
Examiner Name	Seyed H. Azarian
Attorney Docket Number	876564/0083

Sheet 1 of 2

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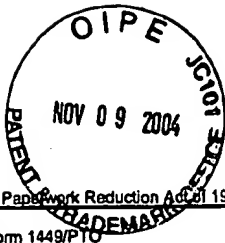
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S.A		"Moment Extraction Architecture for Digital Vision Chip", Technical Report of IEICE, July 1997 (citing the following 12 references).	
		C. Mead and M. Mahowald, "A Silicon Model of Early Visual Processing", Neural Networks, July 1988.	
		M. Ishikawa, A. Morita, and N. Takayanagi, "High Speed Vision System Using Massively Parallel Processing", IROS, 1992.	
		Y. Nakabo, I. Ishii, and M. Ishikawa, "1ms Target Tracking System Using Ultra-Parallel Ultra-High Speed Vision", 1997.	
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		M. Ishikawa, K. Ogawa, T. Komuro, I. Ishii, "A CMOS Vision Chip with SIMD Processing Element Array for 1ms Image Processing", February 1999.	
		T. Bernard, B. Zavidovique, and F. Devos, "A Programmable Artificial Retina", IEEE Journal of Solid-State Circuits", July 1993.	

Examiner Signature	<i>Seyed H. Azarian</i>	Date Considered	<i>6.20.05</i>
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of

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<i>S.A</i>			
✓ ↓		J. Eklund, C. Svensson, and A. Astrom, "VLSI Implementation of a Focal Plane Image Processor...", IEEE Trans. VLSI Systems, September 1996.	
		T. Mukai and M. Ishikawa, "Two-Dimensional Coordinates Transform Circuit for Parallel Processing Vision", Technical Report of IEICE, 1992.	
		I. Ishii, T. Komuro, and M. Ishikawa, "Moment Calculation Method using Bit-Plane Feature Decomposition", Technical Report of IEICE, July 1999.	

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